HARRIS

HD-6121

CMOS I/O CONTROLLER

DISCONTINUED

Features

- LOW POWER, TYP. < 2 mW
- SINGLE SUPPLY – 5V
- INDUSTRIAL AND MILITARY TEMPERATURE RANGES
- 6120 COMPATIBLE INTERFACE
- CONTROLS ANY COMBINATION OF FIVE INPUT OR OUTPUT PORTS WITH HANDSHAKING
- ELIMINATES GATED READ AND WRITE SIGNALS THROUGH THE CONTROLLER
- CONFORMS TO DEC* CONVENTIONS REGARDING DEVICE ADDRESSING AND COMMANDS
- INDEPENDENT PROGRAMMING OF EACH DEVICE'S ADDRESS AND DATA DIRECTION
- COMPLETE INTERRUPT AND SKIP LOGIC FOR EACH DEVICE INCLUDING PRIORITY INTERRUPT VECTORING
- STROBE OUTPUTS ARE PROGRAMMABLE HIGH OR LOW TRUE
- SENSE INPUTS ARE PROGRAMMABLE FOR LEVEL OR EDGE SENSITIVITY
- ENABLE OUTPUTS FUNCTION AS USER PROGRAMMABLE CHIP SELECTS

Description

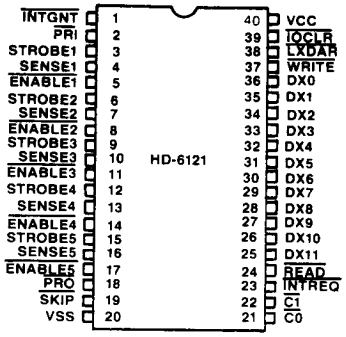
The HD-6121 Input/Output Controller (IOC) is a high performance, CMOS support circuit for the 6120 microprocessor. Fully programmable, this device offers independent control of any combination of five, 12 bit input or output ports.

Used in conjunction with the 6120 microprocessor, the 6121 provides user programmable chip select decoding, priority vectored interrupt control, software readable status and I/O port handshaking signals.

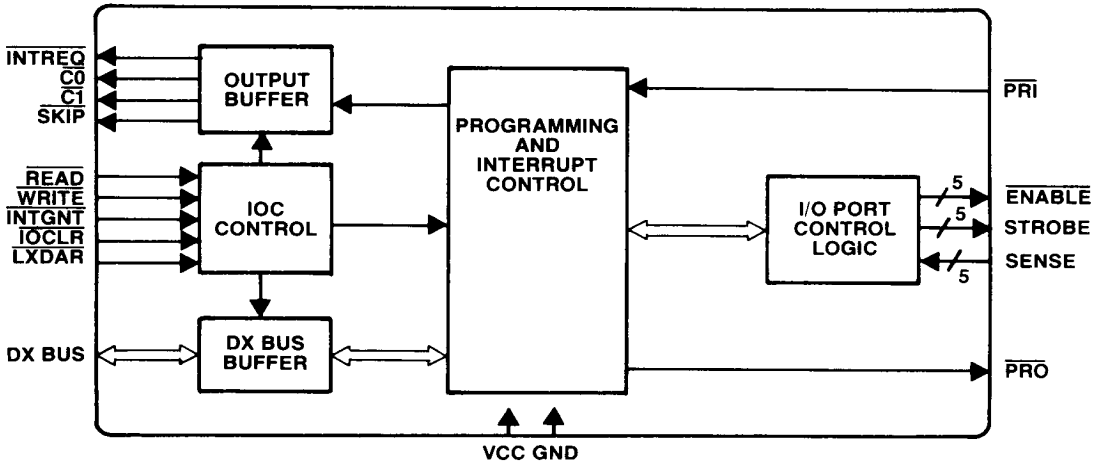
The Priority In ($\overline{PRI}$) and Priority Out ($\overline{PRO}$) control signals permit up to eleven 6121s to be used without any additional hardware. Industrial control and other I/O intensive systems can profit greatly from the highly hardware/software efficient capability provided by the 6120/6121 chip set.

* *TRADEMARK of Digital Equipment Corp.*

Pinout



Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0 VOLTS	Operating Temperature Range	
Operating Voltage Range	+4V to +7V	Industrial (−9, −9+)	−40°C to +85°C
Input/Output Voltage Applied	VSS−0.3V to VCC+0.3V	Military (−2, −8)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	Maximum Power Dissipation	1 Watt

CAUTION: Stresses above those listed in the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. ELECTRICAL CHARACTERISTICS; VCC=5.0V±5%; TA = Industrial or Military

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	LOGICAL ONE INPUT VOLTAGE	70% VCC		V	
VIL	LOGICAL ZERO INPUT VOLTAGE		30% VCC	V	
VOH	LOGICAL ONE OUTPUT VOLTAGE	VCC−0.5		V	IOH = −1.6mA Except for SKIP, INTREQ, C0 and C1 which are open drain.
VOL	LOGICAL ZERO OUTPUT VOLTAGE		0.5	V	IOL = 1.6mA Except for SKIP, INTREQ, C0 and C1.
VOL	LOGICAL ZERO OUTPUT VOLTAGE		0.5	V	IOL = 15 mA SKIP, INTREQ, C0, C1 OUTPUTS
IIL	INPUT LEAKAGE CURRENT	−10	10	μA	OV≤VIN≤VCC
IO	I/O, OUTPUT LEAKAGE CURRENT	−10	10	μA	OV≤VO≤VCC NOTE 1
ICC	POWER SUPPLY CURRENT		100	μA	VIN=VCC or GND VCC = 5.25 V OUTPUTS OPEN
CIN*	INPUT CAPACITANCE		5	pF	FREQ = 1 MHZ TA=25°C VIN=VCC or GND
COUT*	OUTPUT CAPACITANCE		15	pF	FREQ = 1 MHZ TA=25°C VIN=VCC or GND

** Guaranteed and sampled, but not 100% tested*

NOTE 1: APPLIES ONLY TO DX0 THROUGH DX11, C0, C1, SKIP, AND INTREQ WITH THE OUTPUT DRIVERS DISABLED OR OPEN DRAIN OUTPUTS OFF.

A.C. ELECTRICAL CHARACTERISTICS; VCC=5.0V±5%; TA=Industrial or Military; CL=50 pf,

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TAS	ADDRESS SET UP TIME	30		ns	
TAH	ADDRESS HOLD TIME	70		ns	
TRWE	WRITE ENABLE DELAY		100	ns	
TRWD	WRITE DISABLE DELAY		100	ns	
TWS	WRITE SET UP TIME	50		ns	
TWH	WRITE HOLD TIME	50		ns	
TPDE	ENABLE OUTPUT DELAY		125	ns	
TPDD	ENABLE OUTPUT DISABLE DELAY		200	ns	
TRE	READ VECTOR ENABLE		100	ns	
TRD	READ VECTOR DISABLE		100	ns	
TWPD	WRITE PULSE DELAY	100		ns	
TLXH	RESET DELAY, IOCLR TO LXDAR	100		ns	

NOTE: ALL MEASUREMENTS ARE TAKEN WITH INPUT RISE AND FALL TIMES ≤ 20 NSEC

DECOUPLING CAPACITORS

The transient current required to charge and discharge the 50 pf load capacitance specified in the 6121 data sheet is determined by

$$i = C_L\,(dv/dt)$$

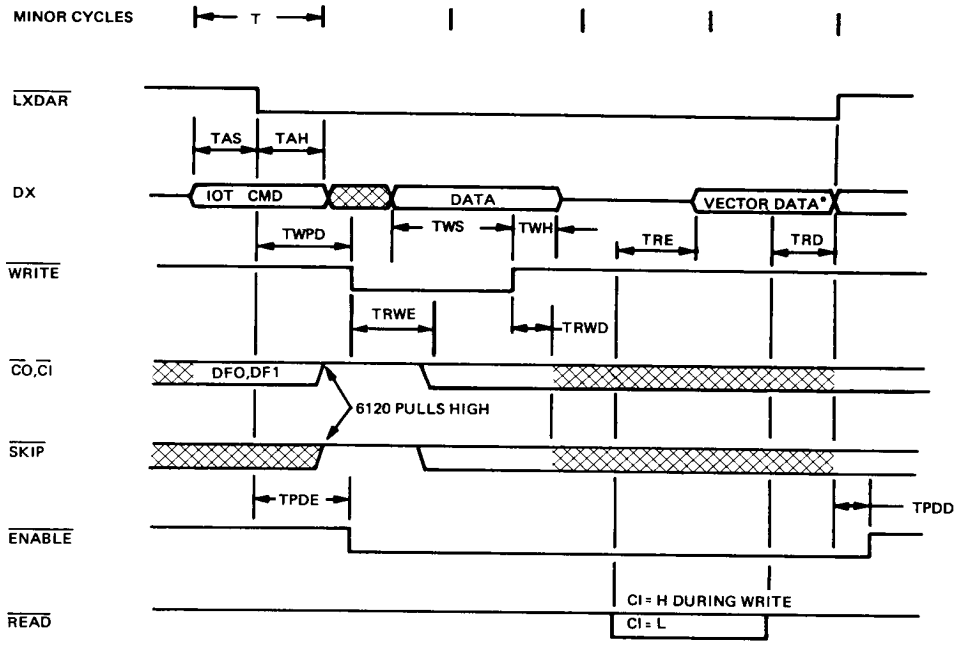
Assuming that all DX outputs change state at the same time and that dv/dt is constant;

$$i \cong C_L \frac{(VCC \times 80\%)}{t_R/t_F}$$

where t_R=20 ns, VCC=5.0 volts, C_L=50 pF on each of twelve outputs.

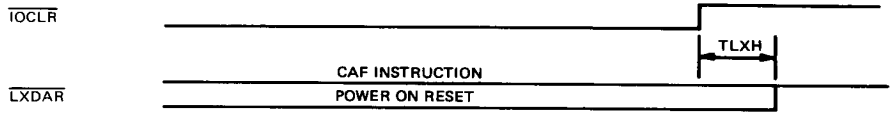
$$i \cong (12 \times 50 \times 10^{-12}) \times (5.0v \times 0.8)/(20 \times 10^{-9})$$
$$\cong 120\ mA$$

This current spike may cause a large negative voltage spike on VCC, which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between VCC and GND at each device, with placement being as near to the device as possible.



* *Vector Operation Only*

EXTERNAL IOT and VECTORED INTERRUPT OPERATION



RESET TIMING

I/O	PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
I	1	$\overline{\text{INTGNT}}$	Low	Interrupt grant signal from the 6120.
I	2	$\overline{\text{PRI}}$	Low	Input for priority string. Low implies no higher priority up the string. Device #1 internally is the highest priority device.
O	3, 6, 9, 12, 15	STROBE 1-5	High or Low	Output strobes set true by a transfer command. Cleared by a Set Flag command or by the corresponding sense input going true. Programmable polarity.
I	4, 7, 10, 13, 16	SENSE 1-5	High or Low	Status inputs from an external device. Can cause IOT skips or interrupts. Programmable edge or level sense and polarity.
O	5, 8, 11, 14, 17	$\overline{\text{ENABLE}}$ 1-5	Low	Bus transfer enable pulses for external devices. True during $\overline{\text{LXDAR}}$.
O	18	$\overline{\text{PRO}}$	Low	Output for priority string. Low implies enable for next device down the string. Device #5 internally is the lowest priority device and drives this output.
O	19	$\overline{\text{SKIP}}$	Low	True during $\overline{\text{LXDAR}}$ and $\overline{\text{WRITE}}$ to indicate to the 6120 that a skip is to occur on the current IOT. N-Channel open drain.
	20	VSS		Power supply ground.
O	21, 22	$\overline{\text{C0}}$, $\overline{\text{C1}}$	Low	Control signals to the 6120 which specify the type of transfer required for an I/O instruction. See Table 1. N-Channel open drain.
O	23	$\overline{\text{INTREQ}}$	Low	Interrupt request to the 6120. N-Channel open drain output.
I	24	$\overline{\text{READ}}$	Low	6120 bus read pulse.
I/O	25-36	DX11-0	High	6120 data/address bus. (DXO=MSB, DX11=LSB)
I	37	$\overline{\text{WRITE}}$	Low	6120 bus write pulse.
I	38	$\overline{\text{LXDAR}}$	Low	6120 I/O transfer enable signal. True during the execute phase of external IOT instruction. Also true during power on reset.
I	39	$\overline{\text{IOCLR}}$	Low	Reset from the 6120 generated by power on reset or CAF instruction.
	40	VCC		Positive supply voltage.

CONCEPT:

The concept of the IOC is to provide basic control and enable signals for the devices which it controls but not be involved in the critical speed timing of the DX bus transfers to and from these devices. Each input or output port still has its own output latch or input driver interface which results in maximum flexibility with regard to I/O device characteristics. Because these latches and input drivers are not included in the 6121, this 40 pin device is able to provide complete handshaking for five I/O ports.

Software programmable chip select decoding ($\overline{\text{ENABLE}}$ outputs) provides a means whereby I/O device addressing is readily changed with no change to the users PC board. This on-chip feature replaces the 2-5 IC's normally associated with chip select decoding.

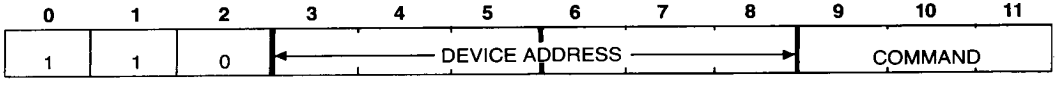
Another feature of the 6121 IOC is an on-chip priority interrupt controller. The interrupt logic includes software programmable vectors and complete interrupt request/grant handshaking for the 6120 microprocessor. This on-chip feature of the 6121 eliminates a separate interrupt controller IC. Up to eleven 6121 IOCs can be daisy chained without the need for any interfacing logic. This results in vectored interrupt control of up to 55 I/O ports. The Priority In ($\overline{\text{PRI}}$) and Priority Out ($\overline{\text{PRO}}$) control signals are used for this I/O expansion capability.

Another major on-chip feature of the 6121 IOC is the inclusion of I/O port handshaking signals. These signals provide the capability of polling the status of an Input port (SENSE inputs) and that of signaling an Output port that it has received data (STROBE outputs). These signals can be thought of as "Input Buffer Full" and "Output Buffer Full" status lines. The characteristics of these signals are software programmable which greatly increases their flexibility.

6120 IOT INSTRUCTION SEQUENCING:

The 6121 is designed to interface with the 6120 external IOT sequence. This sequence begins when the 6120 fetches an instruction from the memory and recognizes that the current instruction is an external IOT. An external IOT is any IOT (Bits 0−2=6) whose device code (Bits 3-8) is not 00 or 2X.

EXTERNAL IOT COMMAND FORMAT



The 6120 sequences the IOT instruction through an execute phase. Bits 0-11 of the IOT instruction are available on DX0-11 as $\overline{LXDAR}$ falls near the start of the execute phase. The 6121 IOC accepts the IOT command on the falling edge of $\overline{LXDAR}$ and latches this information into an internal command latch. $\overline{WRITE}$ or $\overline{READ}$ is active low to enable data transfers between the 6120 and the peripheral device(s). The 6121 communicates with the 6120 through 3 control lines... $\overline{C0}$, $\overline{C1}$ and $\overline{SKIP}$. The type of data transfer during an IOT instruction is specified by the peripheral device by asserting the control lines as shown in Table 1.

The control line $\overline{SKIP}$, when low during an IOT, causes the 6120 to skip the next instruction. This feature is used to sense the status of various signals in the device interface. The $\overline{C0}$ and $\overline{C1}$ lines are treated independently of the $\overline{SKIP}$ line. The input command signals, $\overline{C0}$, $\overline{C1}$ and $\overline{SKIP}$, are sampled during $\overline{LXDAR}$ low • $\overline{WRITE}$ low. The data from the 6120 is available to the device(s) during $\overline{LXDAR}$ low • $\overline{WRITE}$ low. If $\overline{C1}$ is low at $\overline{LXDAR}$ low • $\overline{WRITE}$ low, a read is also performed and data is read from the peripheral into the 6120 during $\overline{LXDAR}$ low • $\overline{READ}$ low.

TABLE 1 – PROGRAMMED I/O CONTROL LINES

CONTROL LINES $\overline{C0}$	$\overline{C1}$	OPERATION	DESCRIPTION
High	High	(Device)◄—(AC)	The contents of the AC is sent to the device.
Low	High	(Device)◄—(AC), Clear (AC)	The contents of the AC is sent to the device, then the AC is cleared.
High	Low	(AC)◄—(AC)V(Device)	Data is received from a device,"OR'ed" with the data in the AC and the result stored in the AC.
Low	Low	(AC)◄—(Device)	Data is received from a device and loaded into the AC.

INTERNAL DEVICE CONTROLLER FLIP FLOP DEFINITIONS:

There are five device controllers within the 6121 IOC. Each controller has a set of control and status flip flops which are defined below:

FLAG FLIP FLOP – Internal device control status flip flop which only has meaning if the IS programming bit is a 1. It is set by a SET FLAG IOT or by true going edge of sense input. It is cleared by the SKIP ON FLAG instruction only if it was sampled by that instruction as being set; by the interrupt vector operation; or by $\overline{IOCLR}$. If the flag is set, interrupts can be generated if otherwise enabled. If the IS programming bit is 0, the flag flip flop is held in the cleared state.

FLAG SAMPLE FLIP FLOP – Internal device control flip flop which samples the state of the flag flip flop at the falling edge of $\overline{LXDAR}$. The set state of this flip flop causes the skip line to be pulled and the flag flip flop to be cleared during $\overline{WRITE}$ pulses of a skip IOT.

STROBE FLIP FLOP – Internal device control flip flop which controls strobe output line. It is set by a transfer IOT at the trailing edge of the $\overline{LXDAR}$ pulse. It is cleared by $\overline{IOCLR}$, the true going edge of the sense input (if the IS programming bit set) or the SET FLAG IOT command. The STROBE output reflects the state of this flip flop any time the strobe flip flop is cleared or at the end of $\overline{LXDAR}$ if the strobe flip flop is set.

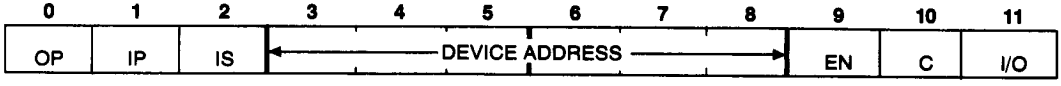
INTERRUPT ENABLE FLIP FLOP – Internal device control flip flop which allows program enable of interrupts. This bit is set by $\overline{IOCLR}$. This bit is loaded by DX11 during $\overline{WRITE}$ of LOAD INTERRUPT ENABLE IOT. If this flip flop and the flag flip flop are both set, then the $\overline{INTREQ}$ pin is pulled low.

INTERRUPT SAMPLE FLIP FLOP – Internal device control flip flop which samples the state of the interrupt condition at the falling edge of $\overline{INTGNT}$. The falling edge of $\overline{INTGNT}$ sets the interrupt sample flip flop if the flag flip flop and interrupt enable flip flop are set and the priority input is true. If the flag flip flop is clear or the priority input is false at the fall of $\overline{INTGNT}$, the state of the interrupt sample flip flop is not changed. The interrupt sample flip flop is cleared by the SKIP ON FLAG IOT, by the reset state of the interrupt enable flip flop or by $\overline{IOCLR}$. If this flip flop is set, the device's priority output is false (high).

PROGRAMMING:

Immediately after power on reset, the five device controllers within the IOC are set to a state such that the first IOT command received with $\overline{PRI}$ low will be interpreted as a programming command to set up various IOC parameters. This is true only for power on reset and is *not* true for the reset generated by the 6120 CAF instruction. Power on reset from the 6120 is distinguished by $\overline{LXDAR}$ being low at the end of the $\overline{IOCLR}$ pulse. During the reset caused by the CAF instruction, $\overline{LXDAR}$ is high throughout the $\overline{IOCLR}$ pulse. Each of the five device controllers within the IOC are programmed independently by separate IOT commands. If PRI is low, the first IOT programs the highest priority device (Device #1). The second IOT programs the second highest priority device (Device #2). This continues until all the devices in the IOC are programmed, at which time $\overline{PRO}$ is made low so that programming can commence on the next IOC (if any) down the priority chain. The IOC will not accept any operational IOT commands to any of the five devices until all five devices have been programmed. The programming IOT writes data from the 6120 accumulator. The lower 9 bits of the IOT instruction itself perform no programming function. The IOT instruction must be an external IOT, not device #00 or 2X. The programming format from the accumulator is shown below:

PROGRAMMING COMMAND FORMAT



OP Output polarity
1=High true strobe output
0=Low true strobe output

IP Input polarity
1=High true sense polarity
0=Low true sense polarity

IS Input edge sensitivity
1=Set flag flip flop and interrupt (if interrupts enabled) on true-going edge of sense input. Skip on flag flip flop set.
0=Skip on sense line input level true. (No interrupt on sense true.)

DEVICE ADDRESS The 6 bit device address assigned to the device controller.

EN Enable output control select.
1=Enable output is true (low) whenever the device is addressed. (Except for programming and vector operations.)
0=Enable is true only when a transfer command (4_8 or 6_8) is given.

C C line control.
0=Transfer commands do not cause C lines to be controlled.
1=Transfer commands cause C lines to be controlled.

I/O Input or output port select. This programming bit has no meaning if the "C" programming bit is set to a "0".
1=Transfer commands cause outputs to the device. ($\overline{C1}$ is not pulled low.)
0=Transfer commands cause inputs from the device. ($\overline{C1}$ is pulled low.)

After all five devices of the IOC are programmed, they are ready to respond to IOT commands with their programmed addresses. Because of this, no operational IOT commands can be used until all system IOC's have been programmed. An additional constraint is that each device must have its own unique address.

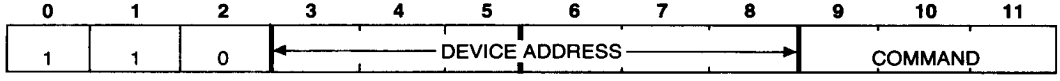
Note that unused devices must be turned off during programming simply by programming them with an internal IOT address (00 or 2X), and with the IS programming bit set to "0" to prevent interrupts. Also, sense inputs must be tied to ground. Internal 6120 IOT's do not generate $\overline{LXDAR}$. The IOT controller is therefore made insensitive to all external IOT commands when programmed with an internal IOT address. Whenever a device controller within the IOC responds to its programming IOT, it pulls the $\overline{C0}$ line low so that the 6120 will perform an output operation from the AC followed by clearing the AC.

IOC COMMANDS:

Power on reset– This is indicated by the $\overline{IOCLR}$ input low and $\overline{LXDAR}$ low at the end of the $\overline{IOCLR}$ pulse. This operation sets up the IOC to be programmed as discussed above. Also, all five flag flip flops are cleared as are the flag sample and interrupt sample flip flops. The interrupt enable flip flops are all set. The strobe flip flops are cleared, the STROBE outputs are set low and the $\overline{ENABLE}$ outputs are set high. Note that if a controller is programmed for a low true STROBE output, then there will be a low to high transition on the strobe output when this device is programmed. Also, care must be taken to assure that the state of the flag, flag sample, interrupt sample, interrupt inhibit and strobe flip flops are *not* disturbed by the programming function.

The 6120 Clear All Flags (CAF) Instruction – This instruction is indicated to the IOC by $\overline{IOCLR}$ going low and $\overline{LXDAR}$ staying high during the $\overline{IOCLR}$ pulse. This operation performs exactly the same operation as power on reset on the device flag, flag sample, interrupt sample, interrupt enable and strobe flip flops. It does not set up the IOC for programming, nor does it disturb the state of any of the programming information stored within the IOC.

EXTERNAL IOT COMMAND FORMAT



	Bit 9	10	11
SET FLAG, CLEAR STROBE	0	0	0
SKIP ON FLAG, CLEAR FLAG	0	0	1
CLEAR ACCUMULATOR (If programmed for input)	0	1	0
NOP	0	1	1
DATA TRANSFER ($\overline{C0}$ not pulled low)	1	0	0
LOAD INTERRUPT ENABLE (From DX11)	1	0	1
DATA TRANSFER ($\overline{C0}$ pulled low)	1	1	0
NOP	1	1	1

Each IOT is discussed below:

SET FLAG, CLEAR STROBE – If the device is programmed for edge sensitive SENSE input, this IOT command causes the internal flag flip flop to be set and also clears the STROBE output to the programmed false state. If the device is programmed for level sensitive SENSE input, then the flag flip flop is not set by this instruction, but the STROBE output is cleared.

SKIP ON FLAG, CLEAR FLAG – The skip on flag operation depends on whether the device is programmed for edge or level sensitivity. If programmed for level sensitivity and the SENSE input is logic true, then the $\overline{SKIP}$ line is pulled low during the IOT $\overline{WRITE}$ pulse; the clear flag operation has no meaning. If programmed for edge sensitivity, then the state of the flag flip flop is sampled to the flag sample flip flop at the falling edge of $\overline{LXDAR}$. During the IOT $\overline{WRITE}$ pulse, the $\overline{SKIP}$ line will be pulled low if the flag sample flip flop is true. If the flag sample flip flop is set, then the flag flip flop will be cleared some time before or at the trailing edge of $\overline{LXDAR}$.

CLEAR ACCUMULATOR – This command only functions if the C line control programming bit (bit 10=1) has been programmed for the device to control the C lines and the device has been programmed as an input device (bit 11=0). When enabled by the above two programming conditions, this command will cause $\overline{C0}$ to be pulled low during the IOT $\overline{WRITE}$ pulse. This will cause the 6120 accumulator to be cleared.

DATA TRANSFER (4_8 or 6_8) – Either transfer command will unconditionally set the STROBE output to its true state. If the "C" programming bit is set, the transfer commands will also cause the "C" lines to be controlled to specify the type of I/O transfer to be performed. If not, then the IOC device does not control the "C" lines. If the device "I/O" programming bit is 1, then $\overline{C1}$ is not pulled low and an output transfer is specified by either 4_8 or 6_8. If the I/O programming bit is 0, then an input transfer is specified by pulling $\overline{C1}$ low during the $\overline{WRITE}$ pulse. Command 4_8 does not pull $\overline{C0}$ low. For an output, this corresponds to not clearing the AC after the output. For an input, this corresponds to "OR'ing" the input data with the AC. Command 6_8 always pulls $\overline{C0}$ low. For an output, this causes the AC to be cleared following the output. For an input, this corresponds to the input data being loaded into the AC. The STROBE output is cleared when the flag flip flop is set by the SENSE transition or by a SET FLAG command.

LOAD INTERRUPT ENABLE – This command causes a write of 6120 AC bit 11 to the addressed device's interrupt enable flip flop. This write holds neither $\overline{C0}$ nor $\overline{C1}$ low so that a write without a clear of the AC is performed. The device is incapable of generating interrupts if the interrupt enable flip flop is cleared.

INTERRUPT LOGIC:

A device controller within the IOC is capable of generating an interrupt by pulling the $\overline{INTREQ}$ line low if all of the following conditions are true:

1. The device is programmed for edge sensitive SENSE input, and
2. The device flag flip flop has been set, and
3. The device interrupt enable flip flop is set, and
4. The priority string input for that device is true.

Normally, with no system interrupts outstanding, all device priority inputs and outputs are low. At the highest priority IOC, the $\overline{PRI}$ input must be tied to Vss.

Whenever the interrupt conditions are met at any device on the IOC, the $\overline{INTREQ}$ line is pulled low and the following sequence of events occurs:

1. The 6120 $\overline{INTREQ}$ being low causes $\overline{INTGNT}$ low. All IOC driving device controllers which have the interrupt condition met set their interrupt sample flip flops. Note that this is an edge triggered *set* and is *not* a "load". All device controllers which have their interrupt sample flip flops set will hold their respective priority outputs high. All device controllers with a high priority input hold their priority outputs high and also are inhibited from driving the $\overline{INTREQ}$ bus low.
2. When the first IOT is executed with $\overline{INTGNT}$ low, one of two events occurs, depending on the IOT command:

a. If the command issued is a SKIP ON FLAG (1_8) command, then the normal operation of the IOT command occurs in the addressed device. A SKIP ON FLAG (1_8) instruction will clear the interrupt sample flip flop of the addressed device and will clear the flag flip flop if it is set.

b. If the command is not a SKIP ON FLAG (1_8) command, then the fact that $\overline{INTGNT}$ is low causes special action. During the $\overline{WRITE}$ pulse $\overline{C0}$ and $\overline{C1}$ are both pulled low by the highest priority device with its interrupt sample flip flop set. No other device (not even the addressed device) will respond on this IOT. This IOT specifies a JAM read cycle. The 6120 then generates a $\overline{READ}$ pulse which causes the device address of the highest priority device with its interrupt sample flip flop set to put its device address on DX6-11 and all zeros on DX0-5. Also, the flag flip flop of that device is cleared, causing it to remove the $\overline{INTREQ}$ drive. The interrupt sample flip flop is not cleared at this time so that the priority output of that device continues to be held false (high).

c. Near the end of the interrupt service routine of that particular device, the software should (with the 6120 interrupts disabled) execute a SKIP ON FLAG IOT to the device. This will clear the interrupt sample flip flop of the device, which in turn will set the priority output of that device true, enabling interrupts from devices lower in the chain.

SOFTWARE NOTES:

1. When performing the interrupt vector operation from the 6120, the accumulator must be loaded with a "no interrupt" vector address (such as zero) before the vector IOT is issued. This vector is left in the accumulator if no internal vector is returned by a device controller.
2. Before a device's interrupts are turned off by resetting its interrupt enable flip flop with a 6XX5 command the 6120's interrupts must be turned off. Failure to do so can result in an unidentifiable interrupt from the device.
3. When turning on a device's interrupt with a 6XX5 command, an immediate interrupt will result if the device's flag is set and the 6120 interrupts are turned on.
4. Because the IOC programming sequence relies on an exact sequence of IOT instructions to be executed and $\overline{IOCLR}$ enables interrupts, the programming instructions must be executed with the 6120's interrupts off.
5. Use of the level sensitive "Skip on Flag, Clear Flag" operation (6xx1), requires that a redundant skip instruction followed by a NOP be used to guarantee that the "Flag Sample Flip Flop" is reset.

TESTING NOTE:

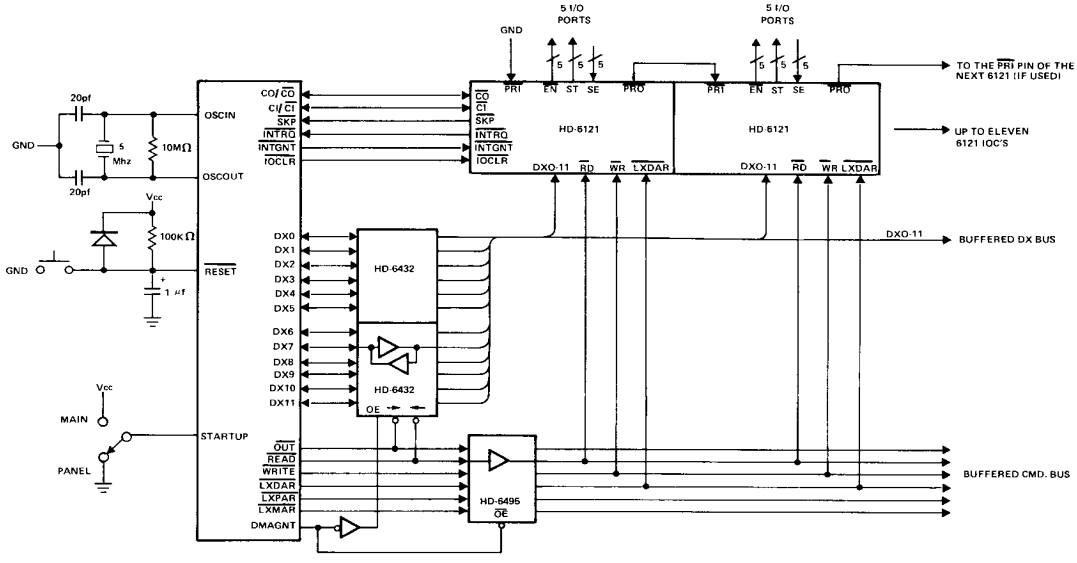
The $\overline{PRO}$ line cannot go true after any $\overline{IOCLR}$ true pulse (either in programming or in a CAF) until there is at least one $\overline{READ}$ pulse. In addition, no external IOT commands can be executed during an $\overline{IOCLR}$ true pulse.

SUMMARY OF 6120, 6121 CONDITIONS:

The following table provides a brief summary of all the 6120 and 6121 Operations.

IOT COMMANDS BIT 9	BIT 10	BIT 11	PROGRAMMING BITS C	I/O	OUTPUTS $\overline{C0}$	$\overline{C1}$	6120 OPERATION	6121 OPERATION
0	1	0	1	1	HiZ	HiZ	Output (AC)	NOP
1	0	0	1	1	HiZ	HiZ	Output (AC)	Generate $\overline{\text{ENABLE}}$. (Output to device.) Set STROBE output.
1	1	0	1	1	Low	HiZ	Output (AC) then (AC)◄— 0	Generate $\overline{\text{ENABLE}}$. (Output to device.) Set STROBE output.
0	1	0	1	0	Low	HiZ	Output (AC) then (AC)◄—0	NOP except for low $\overline{C0}$ output. Result is only to clear 6120 AC.
1	0	0	1	0	HiZ	Low	(AC)◄— Input V(AC)	Generate $\overline{\text{ENABLE}}$. (Input from device.) Set STROBE output.
1	1	0	1	0	Low	Low	(AC)◄— Input	Generate $\overline{\text{ENABLE}}$. (Input from device.) Set STROBE output.
1	0	1	X	X	HiZ	HiZ	Output (AC)	Load interrupt enable flip flop from DX11.
0	0	0	X	X	HiZ	HiZ	Output (AC)	Set flag flip flop if its prog. bit is set. Clear STROBE output.
0	0	1	X	X	HiZ	HiZ	Output (AC)	Pull $\overline{\text{SKIP}}$ low and clear Flag F.F. if flag sample flip flop is a 1 during the write pulse.
X	1	1	X	X	HiZ	HiZ	Output (AC)	No operation.
Vector Read			X	X	Low	Low	(AC)◄— Input	Place interrupt vector on DX bus, clear Flag F.F.
Programming IOT			X	X	Low	HiZ	Output (AC) then (AC)◄— 0	Load programming information to device programming register from the DX bus during write.

BUFFERED BUS 6120/6121 INTERFACING EXAMPLE



NOTE: This simplified example does not show the extended Memory Addressing and other features of the 6120.